said cavity surface being adjacent and in contact with said cavity and said sidewall section, said connection surface being opposite said cavity surface,

said connection surface having a plurality of external electrical connections thereon, an external electrical connection of said plurality of external electrical connections providing a connection to an apparatus external from said semiconductor package,

some external electrical connections of said plurality of external electrical connections being opposite said cavity, and other external electrical connections of said plurality of external electrical connections being opposite said sidewall section.

REMARKS

This is in full and timely response to the non-final Office Action mailed on June 24, 2002. Reexamination in light of the amendments and the following remarks is respectfully requested.

Claims 2, 4 and 7-20 are currently pending in this application, with claims 2, 4, 7, 8 being independent.

No new matter has been added.

Rejections under 35 U.S.C. 112

Claims 2, 3 and 5-8 were rejected under 35 U.S.C. 112, second paragraph.

This rejection is traversed at least for the following reasons.

While not conceding the propriety of this rejection and in order to advance the prosecution of this application, claims 3, 5 and 6 have been canceled and claims 7-8 have been amended, and claims 2, 7 and 8 have been amended. Withdrawal of this rejection and allowance of the claims is respectfully requested.

Rejections under 35 U.S.C. 102 and 103:

Claims 1, 2, 5 and 8 were rejected under 35 U.S.C. 102 as being allegedly anticipated by U.S. Patent No. 5,291,062 issued to Higgins, III (Higgins).

This rejection is respectfully traversed for at least the following reasons.

While not conceding the propriety of these rejections, and in order to further the prosecution of the application, claims 1 and 5 have been canceled without prejudice or disclaimer of their underlying subject matter, rendering moot the rejections as to

these claims.

In addition, claims 2 and 8 have been rewritten in independent form. The features of claim 3 being dependent upon claim 2 as newly added claim 9, and features of claim 6 being dependent upon claim 8 as newly added claim 18.

Claim 2 includes the features of a cavity defined by said first insulating substrate and the sidewall section and encapsulated by encapsulating resin as said semiconductor device is mounted on said mounting portion; and a heat radiating plate is provided on an opposite surface of said first insulating substrate.

Claim 8 includes the steps of encapsulating said cavity with encapsulating resin after mounting said semiconductor device in said mounting portion; and providing a heat radiating plate on the opposite surface of said first insulating substrate after forming said second electrically conductive pattern.

Claims 2 and 8 are deemed clearly anticipated within the non-final Office Action. However, figure 1 of Higgins fails to disclose, teach or suggest a cavity, as claimed. Moreover, figures 3, 4, 6 and 7 of Higgins also fail to teach a cavity encapsulated with encapsulating resin.

Figures 2 and 5 of Higgins arguably teaches an encapsulate within a cavity. However, figures 2 and 5 of Higgins fail to teach a heat radiating plate on the opposite surface of said first insulating substrate.

Furthermore, claim 8 includes the step of providing a heat radiating plate on the opposite surface of said first insulating substrate after forming said second electrically conductive pattern. This step is not found within Higgins.

Thus, Higgins fail to anticipate the claimed invention.

Claims 3, 4, 6 and 7 were rejected under 35 U.S.C. 103 as being allegedly obvious over Higgins.

This rejection is respectfully traversed for at least the following reasons.

While not conceding the propriety of these rejections, and in order to further the prosecution of the application, claims 3 and 6 have been canceled without prejudice or disclaimer of their underlying subject matter.

In addition, claims 4 and 7 have been rewritten in

independent form. The features of claim 3 being dependent upon claim 4 as newly added claim 12, and features of claim 6 being dependent upon claim 7 as newly added claim 15.

Within claims 4 and 7, the first and second insulating substrates, each, are laminated sheets lined with copper. The Office Action correctly admits that these features are not found within Higgins, but asserts, without providing supporting evidence, that these features are well-known.

However, this unsupported assertion amounts to nothing more than conclusions that are personal in nature. Note that the teachings, suggestions or incentives supporting the obviousness-type double patenting rejection must be clear and particular. Broad conclusory statements, standing alone, are not evidence. *In re Dembiczak*, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999).

As a rule, "assertions of technical facts in areas of esoteric technology must always be supported by citation to some reference work recognized as standard in the pertinent art and the appellant given, in the Patent Office, the opportunity to challenge the correctness of the assertion or the notoriety or repute of the cited reference." (Citations omitted). *In re Pardo and Landau*, 214 USPQ 673, 677 (CCPA 1982). The support must have existed at the time the claimed invention was made. *In re Merck &*

Co., Inc., 231 USPQ 375, 379 (Fed. Cir. 1986).

"Allegations concerning specific 'knowledge' of the prior art, which might be peculiar to a particular art should also be supported and the appellant similarly given the opportunity to make a challenge." (Citations omitted). *In re Pardo and Landau*, 214 USPQ 673, 677 (CCPA 1982).

In addition, "it is impermissible, however, simply to engage in a hindsight reconstruction of the claimed invention, using the applicant's structure as a template and selecting elements from references to fill the gaps. The references themselves must provide some teaching whereby the applicant's combination would have been obvious" (citations omitted). *In re Gorman*, 18 USPQ2d 1885, 1888 (Fed. Cir. 1991). See also *In re Dembiczak*, 50 USPQ2d 1614, 1616 (Fed. Cir. 1999)(rejection based upon hindsight is reversed).

Moreover, the procedures established by Title 37 of the Code of Federal Regulations expressly entitle the Applicant to an Examiner's affidavit upon request. Specifically, "when a rejection in an application is based on facts within the personal knowledge of an employee of the Office, the data shall be as specific as possible, and the reference must be supported, when called for by the applicant, by the affidavit of such employee,

and such affidavit shall be subject to contradiction or explanation by the affidavits of the applicant and other persons." 37 C.F.R. 1.104(d)(2).

Also note that the failure to provide any objective evidence to support the challenged use of Official Notice constitutes **clear and reversible error**. *Ex parte Natale*, 11 USPQ2d 1222, 1227-1228 (Bd. Pat. App. & Int. 1989).

Accordingly, **Applicant hereby requests a reference or an Examiner's affidavit** to support this officially noticed position of obviousness or what is well known.

Further note that if this reference or Examiner's affidavit is not provided, the assertions of what is well known **must be withdrawn**. See M.P.E.P. 2144.03.

In addition, this assertion amounts to nothing more than an "obvious-to-try" situation. Specifically, "an 'obvious-to-try' situation exists when a general disclosure may pique the scientist's curiosity, such that further investigation might be done as a result of the disclosure, but the disclosure itself does not contain a sufficient teaching of how to obtain the desired result, or that the claimed result would be obtained if certain directions were pursued." *In re Eli Lilly & Co.*, 14

USPQ2d 1741, 1743 (Fed. Cir. 1990). Moreover, "an invention is 'obvious to try' where the prior art gives either no indication of which parameters are critical or no direction as to which of many possible choices is likely to be successful." *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 10 USPQ2d 1843, 1845 (Fed. Cir. 1989).

Here, Higgins does not contain a sufficient teaching of how to obtain the desired result, or that the claimed result would be obtained if certain directions were pursued. "Obvious to try" is not the standard under §103. *In re O'Farrell*, 7 USPQ2d 1673, 1680 (Fed. Cir. 1988).

New non-final Office Action

If the allowance of claims 2, 4, 7 and 8 is not forthcoming at the very least, then a **new non-final Office Action** is respectfully requested.

Conclusion

For the foregoing reasons, all the claims now pending in the present application are allowable, and the present application is in condition for allowance. Accordingly, favorable reexamination and reconsideration of the application in light of the amendments and remarks is courteously solicited.

If the Examiner has any comments or suggestions that could place this application in even better form, the Examiner is requested to telephone Brian K. Dutton, Reg. No. 47,255, at 202-955-8753, or the undersigned attorney at the below-listed number.

Respectfully submitted,

47,255

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DATE: September 24, 2002

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APPENDIX

IN THE CLAIMS

Please cancel claims 1, 3, 5 and 6 without prejudice or disclaimer of their underlying subject matter.

1. (canceled).

2. (amended) A semiconductor package comprising:

a first insulating substrate carrying a mounting portion for mounting a semiconductor device and a first electrically conductive pattern electrically connected to said semiconductor device;

a sidewall section formed upright around said mounting portion of said first insulating substrate;

a cavity defined by said first insulating substrate and the sidewall section and encapsulated by encapsulating resin as said semiconductor device is mounted on said mounting portion; and

a second insulating substrate provided in said cavity and on said sidewall section and carrying a second electrically conductive pattern electrically connected to said first electrically conductive pattern via through-holes formed in said sidewall section;

wherein solder lands are provided at least in said cavity on one surface of said first insulating substrate,

~~The semiconductor package according to claim 1~~ wherein a heat radiating plate is provided on ~~the~~ an opposite surface of said first insulating substrate.

3. (canceled).

4. (amended) A semiconductor package comprising:

a first insulating substrate carrying a mounting portion for mounting a semiconductor device and a first electrically conductive pattern electrically connected to said semiconductor device;

a sidewall section formed upright around said mounting portion of said first insulating substrate;

a cavity defined by said first insulating substrate and the sidewall section and encapsulated by encapsulating resin as said semiconductor device is mounted on said mounting portion; and

a second insulating substrate provided in said cavity and on said sidewall section and carrying a second electrically conductive pattern electrically connected to said first electrically conductive pattern via through-holes formed in said sidewall section;

wherein solder lands are provided at least in said cavity on one surface of said first insulating substrate,

~~The semiconductor package according to claim 1~~ wherein said second insulating substrate is a laminated sheet lined on one side with copper.

5. (canceled).

6. (canceled).

7. (amended) A method for the preparation of a semiconductor package comprising the steps of:

forming a mounting portion for mounting a semiconductor device and a first electrically conductive pattern for electrically connecting the semiconductor device on a first insulating substrate;

layering a spacer having an opening of substantially the same size as said mounting portion in one surface of said first insulating substrate;

mounting a semiconductor device in said mounting portion defined by said first insulating substrate and the opening provided in said spacer;

encapsulating said cavity with encapsulating resin after mounting said semiconductor device in said mounting portion;

layering a second insulating substrate carrying the a second electrically conductive pattern on one surface thereof on said spacer;

forming a through-hole for establishing electrical connection between said first electrically conductive pattern and said second electrically conductive pattern; and

forming solder lands at least on said cavity on said electrically conductive pattern,

~~The method according to claim 5~~ wherein said second insulating substrate is a laminated sheet lined on one side with copper.

8. (amended) A method for the preparation of a semiconductor package comprising the steps of:

forming a mounting portion for mounting a semiconductor device and a first electrically conductive pattern for electrically connecting the semiconductor device on a first insulating substrate;

layering a spacer having an opening of substantially the same size as said mounting portion in one surface of said first insulating substrate;

mounting a semiconductor device in said mounting portion defined by said first insulating substrate and the opening provided in said spacer;

encapsulating said cavity with encapsulating resin after mounting said semiconductor device in said mounting portion;

layering a second insulating substrate carrying the a second electrically conductive pattern on one surface thereof on said spacer;

forming a through-hole for establishing electrical connection between said first electrically conductive pattern and said second electrically conductive pattern;

forming solder lands at least on said cavity on said electrically conductive pattern; and ~~The method according to claim 5 further comprising:~~

providing a heat radiating plate on the opposite surface of said first insulating substrate after forming said second electrically conductive pattern.

Please add the following new claims.

9. (new) The semiconductor package according to claim 2, wherein said first insulating substrate is a laminated sheet lined on both sides of the insulating substrate with copper.

10. (new) The semiconductor package according to claim 2, wherein said encapsulating resin is planarized.

11. (new) The semiconductor package according to claim 2, wherein said second insulating substrate includes a cavity surface and a connection surface,

said cavity surface being adjacent and in contact with said cavity and said sidewall section, said connection surface being opposite said cavity surface,

said connection surface having a plurality of external electrical connections thereon, an external electrical connection of said plurality of external electrical connections providing a connection to an apparatus external from said semiconductor package,

some external electrical connections of said plurality of external electrical connections being opposite said cavity, and other external electrical connections of said plurality of external electrical connections being opposite said sidewall section.

12. (new) The semiconductor package according to claim 4, wherein said first insulating substrate is a laminated sheet lined on both sides of the insulating substrate with copper.

13. (new) The semiconductor package according to claim 4, wherein said encapsulating resin is planarized.

14. (new) The semiconductor package according to claim 4, wherein said second insulating substrate includes a cavity surface and a connection surface,

said cavity surface being adjacent and in contact with said cavity and said sidewall section, said connection surface being opposite said cavity surface,

said connection surface having a plurality of external electrical connections thereon, an external electrical connection of said plurality of external electrical connections providing a connection to an apparatus external from said semiconductor package,

some external electrical connections of said plurality of external electrical connections being opposite said cavity, and other external electrical connections of said plurality of external electrical connections being opposite said sidewall section.

15. (new) The method according to claim 7, wherein said first insulating substrate is a laminated sheet lined on both sides of the insulating substrate with copper.

16. (new) The method according to claim 7, wherein said encapsulating resin is planarized prior to said step of layering said second insulating substrate.

17. (new) The method according to claim 7, wherein said second insulating substrate includes a cavity surface and a connection surface,

said cavity surface being adjacent and in contact with said cavity and said sidewall section, said connection surface being opposite said cavity surface,

said connection surface having a plurality of external electrical connections thereon, an external electrical connection of said plurality of external electrical connections providing a connection to an apparatus external from said semiconductor package,

some external electrical connections of said plurality of external electrical connections being opposite said cavity, and other external electrical connections of said plurality of external electrical connections being opposite said sidewall section.

18. (new) The method according to claim 8, wherein said first insulating substrate is a laminated sheet lined on both sides of the insulating substrate with copper.

19. (new) The method according to claim 8, wherein said encapsulating resin is planarized prior to said step of layering said second insulating substrate.

20. (new) The method according to claim 8, wherein said second insulating substrate includes a cavity surface and a connection surface,

said cavity surface being adjacent and in contact with said cavity and said sidewall section, said connection surface being opposite said cavity surface,

said connection surface having a plurality of external electrical connections thereon, an external electrical connection of said plurality of external electrical connections providing a connection to an apparatus external from said semiconductor package,

some external electrical connections of said plurality of external electrical connections being opposite said cavity, and other external electrical connections of said plurality of external electrical connections being opposite said sidewall section.